LG Display

LC490DGJ

Product Specification

SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	49.0" QWUXGA TFT LCD

BUYER	General
SET MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LC490DGJ
SUFFIX	SLA1 (RoHS Verified)

APPROVED BY	SIGNATURE DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
YoonSan Park / Team Leader	
REVIEWED BY	
ByungJin Choi / Project Leader	
PREPARED BY	
Dongmin Lee / Engineer	

TV Product Development Dept.
LG Display Co., Ltd.

Ver. 1.0

2017-11-17 08:39:21 dongmin LG Display

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RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	Jul, 14, 2017	-	Preliminary Specification (First Draft)
0.2	Sep. 05. 2017	6	Electrical Characteristics update
		11	Power Sequence update
		12	Optical Specification update
		17	Board Assembly Dimension update
		28	Appendix - Ⅴ Flicker Adjustment update
		29	Appendix - Ⅵ EQ Mode update
1.0	Nov. 17. 2017	5	Electrical Specifications update
		7,8	LCD Connector update
		9	Signal Timing Specifications update
		12	Optical Specification update
		17	Mechanical Dimension update

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1. General Description

The LC490DGJ is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element.
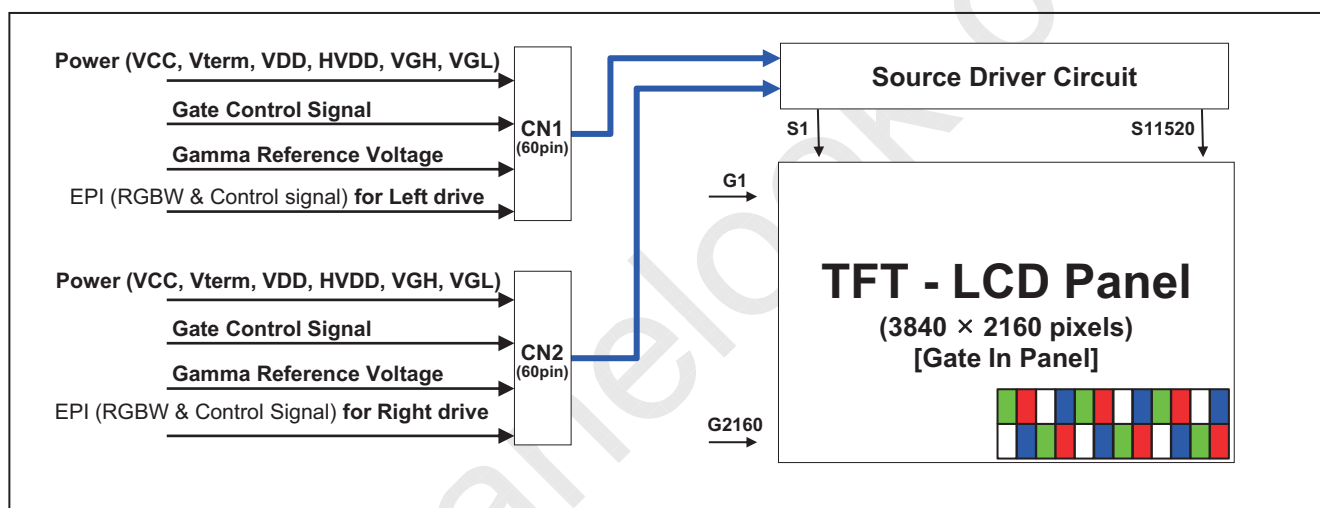It is a transmissive type display operating in the normally black mode. It has a 48.50 inch diagonally measured active display area with QWUXGA resolution (2160 vertical by 3840 horizontal pixel array).
Sub-pixels are constructed with Red, Green, Blue and White. Each pixel is divided into RGB or WRG or BWR or GBW or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 1.07Bilion colors.
It has been designed to apply the 10-bit 8 Lane V by One interface.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.

Power (VCC, Vterm, VDD, HVDD, VGH, VGL)

Gate Control Signal

Gamma Reference Voltage

EPI (RGBW & Control signal) **for Left drive**

CN1 (60pin)

Power (VCC, Vterm, VDD, HVDD, VGH, VGL)

Gate Control Signal

Gamma Reference Voltage

EPI (RGBW & Control Signal) **for Right drive**

CN2 (60pin)

Source Driver Circuit

S1   S11520

G1

TFT - LCD Panel
(3840 × 2160 pixels)
[Gate In Panel]

G2160

General Features

Active Screen Size	48.50 inches(1232.0mm) diagonal
Outline Dimension	1085.5 (H) x 617.7 (V) x 1.2 (D) mm(Typ.)
Pixel Pitch	0.27963 mm x 0.27963 mm
Pixel Format	3840 horiz. by 2160 vert. Pixels,
Power Consumption	Total 258W(Typ)
Luminanc,White	2500cd/ (Centernal point,Typ)
Transmittance (With POL)	7.49% (Typ)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Weight	2.0Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment (Top)	Hard coating(2H), Anti-glare low reflection treatment of the front polarizer (Haze 3%(Typ.))

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2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

| Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic & EPI Power Voltage	VCC	-0.5	+2.2	V_{DC}	1
Gate High Voltage	VGH	+18.0	+30.0	V_{DC}	
Gate Low Voltage	VGL1	-8.0	-4.0	V_{DC}	
	VGL2	-16.0	-4.0	V_{DC}	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	V_{DC}	
Gamma Ref. Voltage (Upper)	VGMH	½VDD-0.3	VDD+0.5	V_{DC}	
Gamma Ref. Voltage (Low)	VGML	-0.3	½ VDD+0.3	V_{DC}	
Panel Front Temperature	TSUR	-	+68	°C	4
Operating Temperature	TOP	0	+50	°C	2,3
Storage Temperature (without packing)	TST	-20	+60	°C	
Operating Ambient Humidity	HOP	10	90	%RH	
Storage Humidity	HST	5	90	%RH	

Notes 1. Ambient temperature condition (Ta = 25 ± 2 °C)
2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39°C, and no condensation of water.
3. Gravity mura can be guaranteed below 40°C condition.
4. The maximum operating temperatures is based on the test condition that the surface temperature of display area is less than or equal to 68°C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68℃. The range of operating temperature may be degraded in case of improper thermal management in final product design.
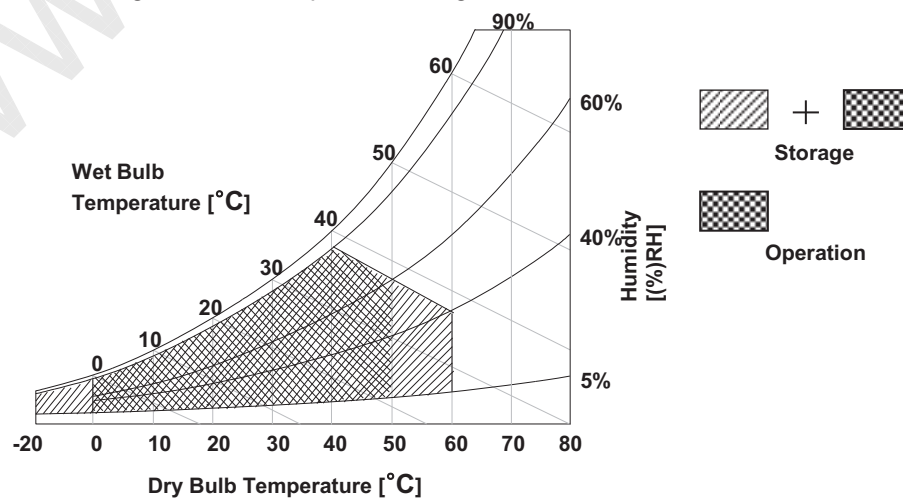
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3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic & EPI Power Voltage	VCC	-	1.78	1.88	1.98	VDC	
Logic High Level Input Voltage	V_{IH}	-	0.8VCC	-	VCC	VDC	
Logic Low Level Input Voltage	V_{IL}	-	0	-	0.2VCC	VDC	
Source D-IC Analog Voltage	VDD	-	14.8	15.0	15.2	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	7.1	7.3	7.5	VDC	7
Gamma Reference Voltage	V_{GMH}	(GMA1 ~ GMA9)	H_VDD+0.2V	-	VDD-0.2	VDC	
	V_{GML}	(GMA10 ~ GMA18)	0.2	-	H_VDD-0.2V	VDC	
Common Voltage	Vcom	Reverse	3.72	4.22	4.72	V	
Vterm	Vterm	CML Type Vcore_tx=1.0V ~ 1.2V	Vcore_Tx - 10%	Vcore_Tx	Vcore_Tx +10%	V	6
EPI input common voltage	VCM	CML Type	0.75		Vterm – Vdiff/2	V	
EPI input differential voltage	Vdiff	-	150	-	500	mV	
EPI Input eye diagram	Veye	-	90	-	-	mV	
Gate High Voltage	VGH	@ 25℃	27.7	28	28.3	VDC	
		@ 0℃	29.7	30	30.3	VDC	
Gate Low Voltage	VGL1	-	-7.2	-7.0	-6.8	VDC	
	VGL2	-	-15.2	-15.0	-14.8	VDC	
GIP Refresh Voltage	VGH even/odd	-	VGL2	-	VGH	V	
GIP Start Pulse Voltage	VST	-	VGL2	-	VGH	V	
GIP Operating Clock	GCLK	-	VGL2	-	VGH	V	
Total Power Current	I_{LCD}	-	-	940	1220	mA	1
		-	-	1520	1980	mA	2
Total Power Consumption	P_{LCD}	-	-	11.9	15.5	Watt	1

Note:

1. The specified current and power consumption are under the VLCD=12.7V., 25 ± 2°C, f_V=60Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The above spec is based on the basic model.
4. All of the typical gate voltage should be controlled within 1% voltage level
5. Ripple voltage level is recommended under ±5% of typical voltage
6. In case of EPI signal spec, refer to Fig 2 for the more detail.
7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10.
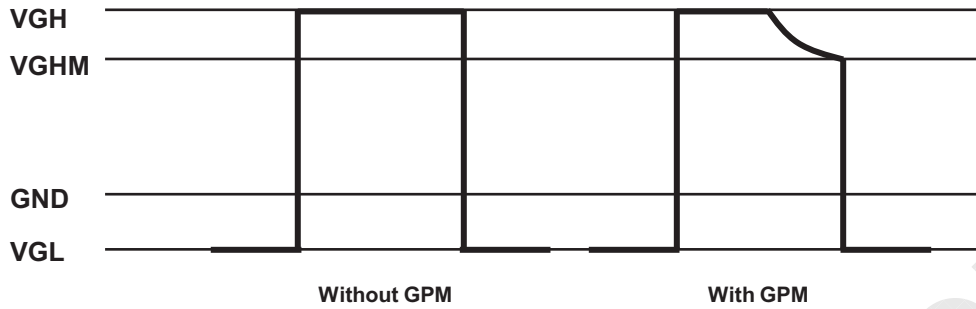
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VGH
VGHM

GND
VGL

Without GPM   With GPM

FIG. 1 Gate Output Wave form without GPM and with GPM

V_{diff}

0 V

V_{diff}

(Differential Probe)

EPI +

V_{diff}

EPI -

V_{cm}

0 V

(Active Probe)
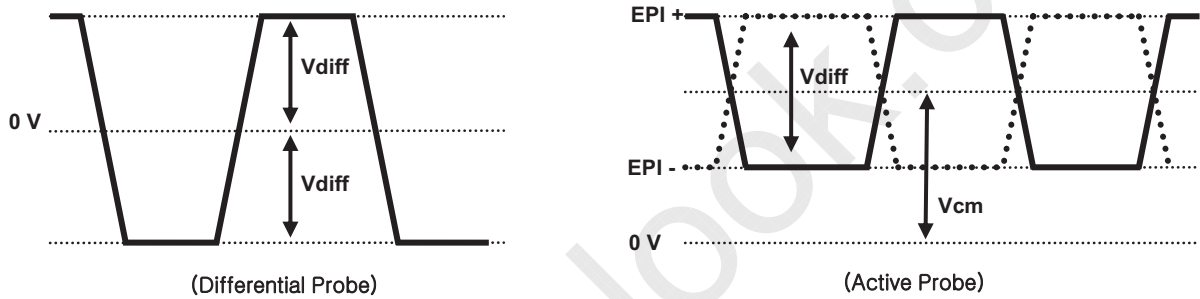
FIG. 2-1 EPI Differential signal characteristics

1 UI

0.5 UI

0 V

V_{eye}

V_{eye}

B1   B2
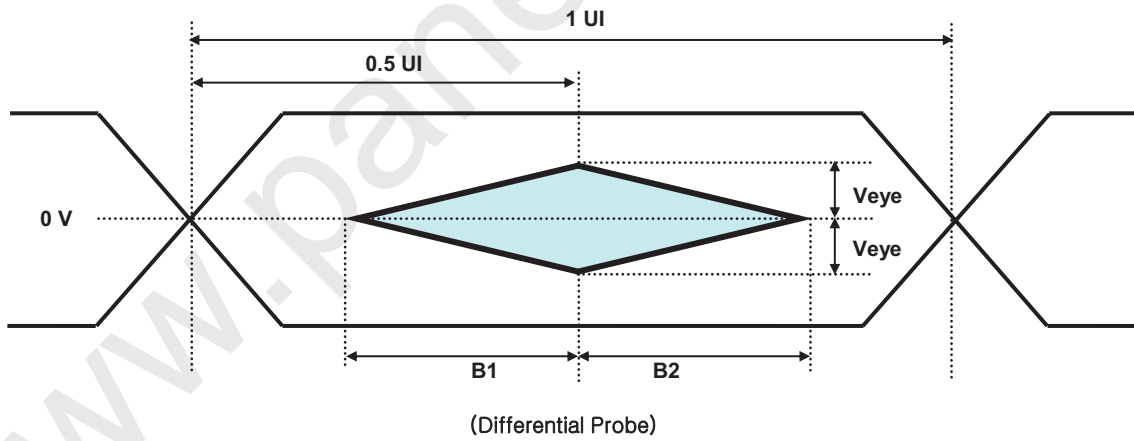
(Differential Probe)

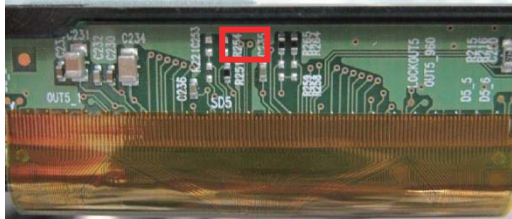**FIG. 2-2 Eye Pattern of EPI Input**

*Source PCB

FIG. 3 Measure point

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3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics and 7-pin connector is used for the integral backlight system.

3-2-1. LCD Module

- LCD Connector(CN1): TF49-60S-0.5SH(manufactured by HIROSE) or compatible

Table 3-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	CLK1	GIP GATE Clock 1	31	GND	Ground
2	CLK2	GIP GATE Clock 2	32	NC	No Connection
3	CLK3	GIP GATE Clock 3	33	NC	No Connection
4	CLK4	GIP GATE Clock 4	34	GND	Ground
5	CLK5	GIP GATE Clock 5	35	EPI3-	EPI Receiver Signal(3-)
6	CLK6	GIP GATE Clock 6	36	EPI3+	EPI Receiver Signal(3+)
7	CLK7	GIP GATE Clock 7	37	GND	Ground
8	CLK8	GIP GATE Clock 8	38	EPI2-	EPI Receiver Signal(2-)
9	CLK9	GIP GATE Clock 9	39	EPI2+	EPI Receiver Signal(2+)
10	CLK10	GIP GATE Clock 10	40	GND	Ground
11	VGH	Gate High Voltage	41	EPI1-	EPI Receiver Signal(1-)
12	BRST	GIP Panel VDD for GATE TFT	42	EPI1+	EPI Receiver Signal(1+)
13	NC	No Connection	43	GND	Ground
14	VGL2	Gate Low Voltage 2	44	GMA18	GAMMA VOLTAGE 18
15	GIP_RESET	Reset Signal for GIP	45	GMA15	GAMMA VOLTAGE 15
16	VST	Vertical Start Pulse	46	GMA14	GAMMA VOLTAGE 14
17	VGL1	Gate Low Voltage 1	47	GMA13	GAMMA VOLTAGE 13
18	VCOM2_L	VCOM Left Bottom Input	48	GMA10	GAMMA VOLTAGE 10
19	VCOM_L_FB	VCOM Left Feed-Back Output	49	GMA9	GAMMA VOLTAGE 9
20	VCOM1_L	VCOM Left Top Input	50	GMA6	GAMMA VOLTAGE 6
21	GND	Ground	51	GMA5	GAMMA VOLTAGE 5
22	VDD	Driver Power Supply Voltage	52	GMA4	GAMMA VOLTAGE 4
23	VDD	Driver Power Supply Voltage	53	GMA1	GAMMA VOLTAGE 1
24	VDD	Driver Power Supply Voltage	54	FLASH_WP	Flash memory Write Protection
25	VDD	Driver Power Supply Voltage	55	FLASH_DO	Flash memory DO
26	HVDD	Half Driver Power Supply Voltage	56	FLASH_CS	Flash memory CS
27	VCC18	Logic & EPI Power Voltage	57	FLASH_DI	Flash memory DI
28	VCC18	Logic & EPI Power Voltage	58	GND	Ground
29	Vterm	Vterm Power Voltage	59	FLASH_CLK	Flash memory CLK
30	LOCK_O	LOCKOUT3	60	VCC33	Flash memory Power Voltage

Note :   1. Please refer to application note for details. (**GIP** & **Half VDD & Gamma Voltage setting**)

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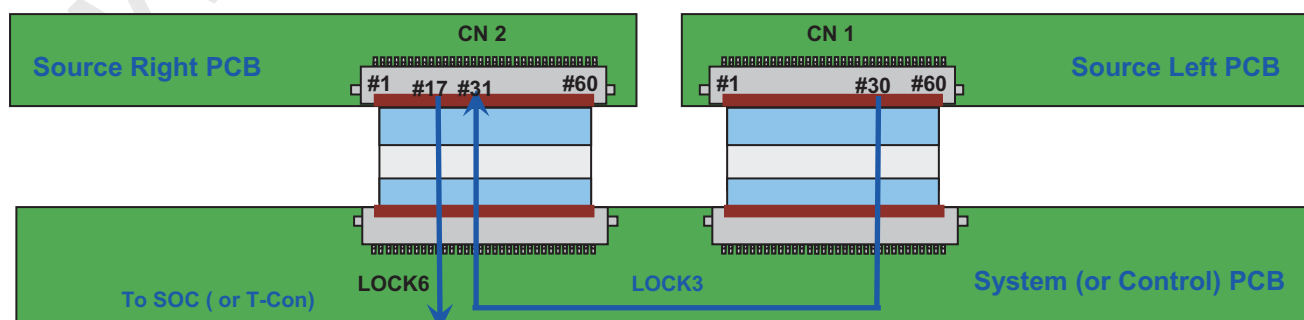
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- LCD Connector(CN2): TF49-60S-0.5SH(manufactured by HIROSE) or compatible

Table 3-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VCC33	EEPROM Power Voltage	31	LOCK_I	LOCKIN3
2	SDA	SDA(I2C)	32	Vterm	Vterm Power Voltage
3	SCL	SCL(I2C)	33	VCC18	Logic & EPI Power Voltage
4	WP	EEPROM Write Protection	34	VCC18	Logic & EPI Power Voltage
5	GND	Ground	35	HVDD	Half Driver Power Supply Voltage
6	GMA18	GAMMA VOLTAGE 18	36	VDD	Driver Power Supply Voltage
7	GMA15	GAMMA VOLTAGE 15	37	VDD	Driver Power Supply Voltage
8	GMA14	GAMMA VOLTAGE 14	38	VDD	Driver Power Supply Voltage
9	GMA13	GAMMA VOLTAGE 13	39	VDD	Driver Power Supply Voltage
10	GMA10	GAMMA VOLTAGE 10	40	GND	Ground
11	GMA9	GAMMA VOLTAGE 9	41	VCOM1_R	VCOM Right Top Input
12	GMA6	GAMMA VOLTAGE 6	42	VCOM_R_FB	VCOM Right Feed-Back Output
13	GMA5	GAMMA VOLTAGE 5	43	VCOM2_R	VCOM Right Bottom Input
14	GMA4	GAMMA VOLTAGE 4	44	VGL1	Gate Low Voltage 1
15	GMA1	GAMMA VOLTAGE 1	45	VST	Vertical Start Pulse
16	GND	Ground	46	GIP_RESET	Reset Signal for GIP
17	LOCK_O	LOCKOUT6	47	VGL2	Gate Low Voltage 2
18	GND	Ground	48	NC	No Connection
19	EPI6-	EPI Receiver Signal(6-)	49	BRST	GIP Panel VDD for GATE TFT
20	EPI6+	EPI Receiver Signal(6+)	50	VGH	Gate High Voltage
21	GND	Ground	51	CLK10	GIP GATE Clock 10
22	EPI5-	EPI Receiver Signal(5-)	52	CLK9	GIP GATE Clock 9
23	EPI5+	EPI Receiver Signal(5+)	53	CLK8	GIP GATE Clock 8
24	GND	Ground	54	CLK7	GIP GATE Clock 7
25	EPI4-	EPI Receiver Signal(4-)	55	CLK6	GIP GATE Clock 6
26	EPI4+	EPI Receiver Signal(4+)	56	CLK5	GIP GATE Clock 5
27	GND	Ground	57	CLK4	GIP GATE Clock 4
28	NC	No Connection	58	CLK3	GIP GATE Clock 3
29	NC	No Connection	59	CLK2	GIP GATE Clock 2
30	GND	Ground	60	CLK1	GIP GATE Clock 1

Note : Please refer to application note for details.
(**GIP** & **Half VDD & Gamma Voltage setting**)

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3-3. Signal Timing Specifications

Table 4. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	notes
Unit Interval	UI	-	0.33	-	0.67	ns	
Effective Veye width time	B1&B2	-	0.25	-	-	UI	Fig. 2
Modulation Ratio of SSC	Vspread	@100KHz	-	-	1	%	1
1st data to SOE rising time	Ts1	-	3	-	-	Packet	Fig.4
SOE rising to last data	Ts4		0	-	-	Packet	Fig.4
Last data to SOE falling	Ts5	-	10	-	-	Packet	Fig.4
EPI Bandwidth	BW	-	2.0	-	3.05	GBPS	

notes : 1. VModulation Ratio of SSC for 20KHz ~ 100kHz Modulation Frequency is calculated by
(3 – 0.02*Fmod), where Fmod unit is KHz.

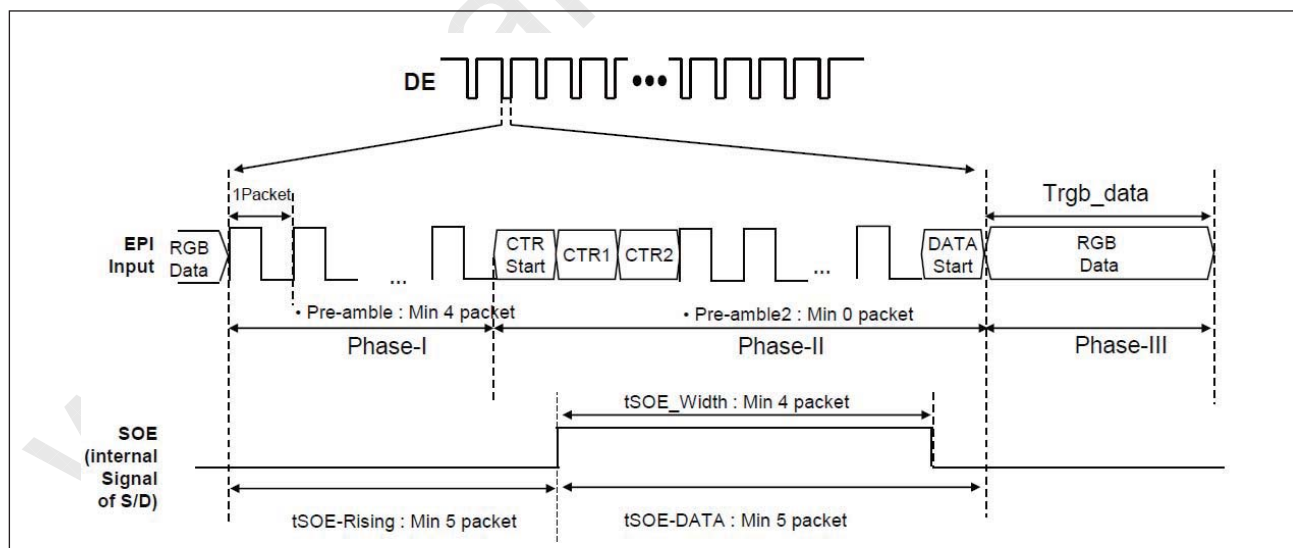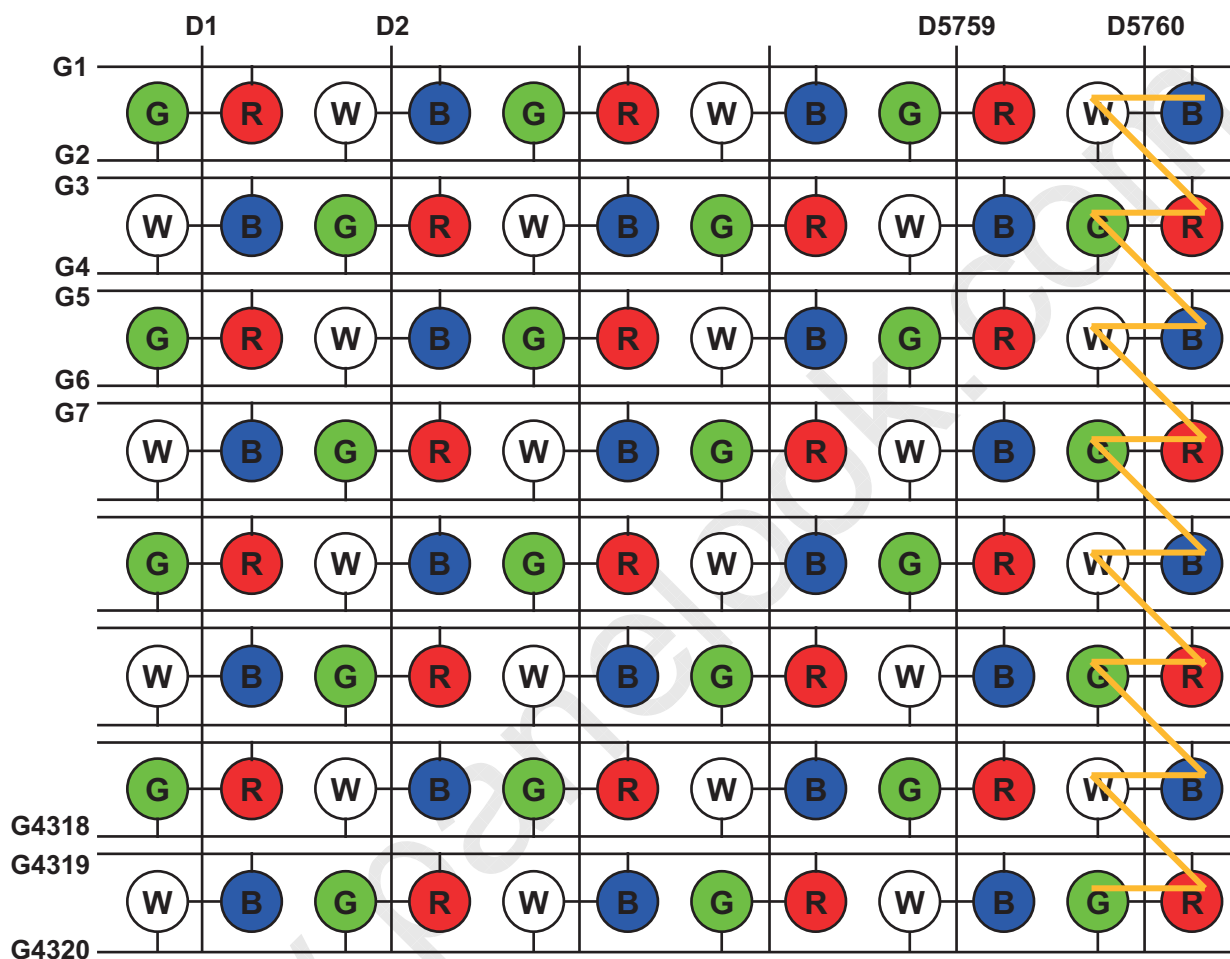
FIG 4. SOE Width & Timing

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3-4. Panel Pixel Structure

FIG. 5 Panel Pixel Structure

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3-5. Power Sequence

3-5-1. LCD Driving circuit

Power Supply For LCD VCC

Power Supply For LCD
VDD, HVDD,VGH, Gamma Ref.
Voltage

Power Supply For LCD
VGL

GIP Signal For LCD

Power For LED
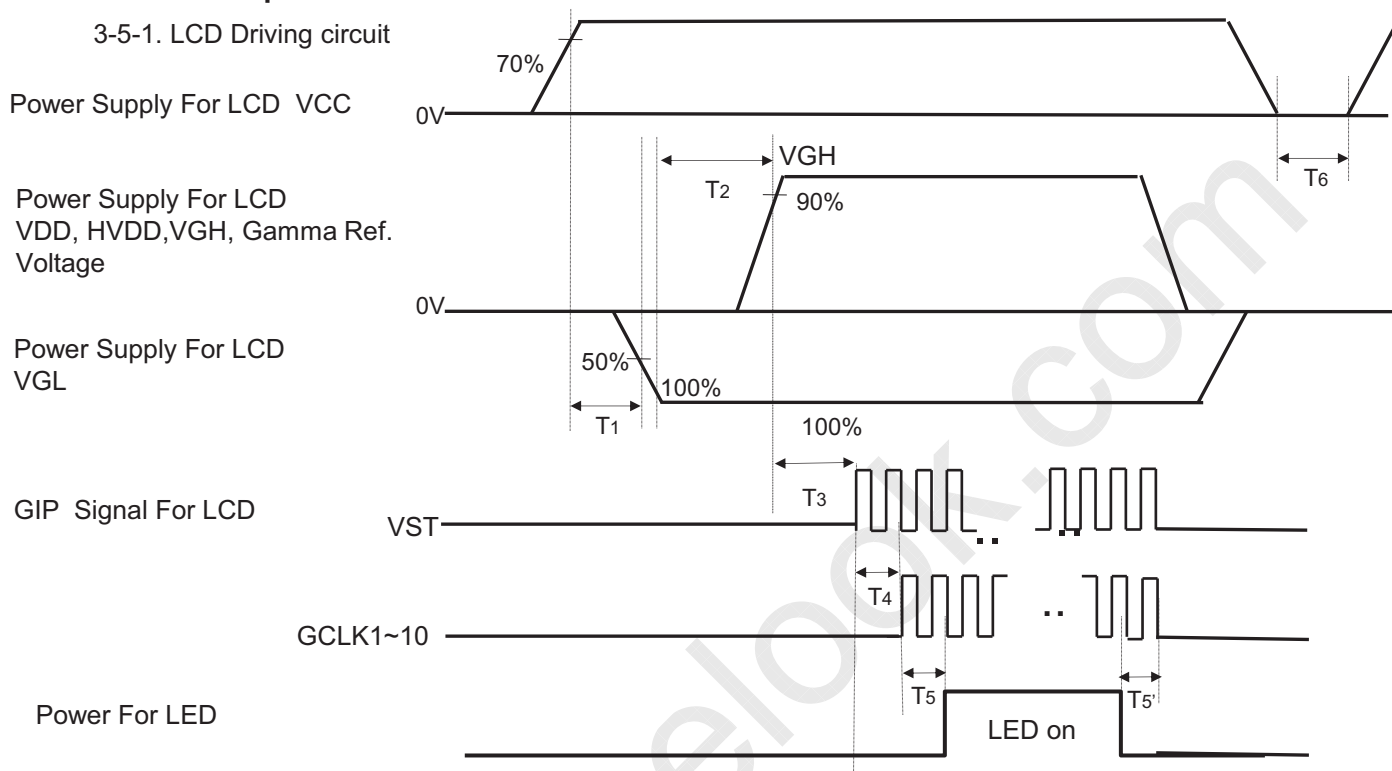
Table 6. POWER SEQUENCE   Ta= 25±2°C, fv=60Hz,

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T_1	0.5	-	-	ms	
T_2	0.5	-	-	ms	
T_3	10	-	-	ms	
T_4	0	-	-	ms	3
T_5 / T_5'	20	-	-	ms	4
T_6	2	-	-	s	

Note : 1. Power sequence for Source D-IC must follow the Case1 & 2.
　　　※ Please refer to Appendix IV for more details.
　　2. During blank period, BRST need to high, during data period BRST need to low.
　　3. GCLK On Sequence : After dummy 5ea (GCLK5 ~ GCLK1), Active GCLK10.
　　: GCLK5 → GCLK4 →GCLK3 → GCLK2 → GCLK1 → GCLK10 → GCLK9 → GCLK8 → GCLK7 → GCLK6.
　　　GCLK off Sequence : No Dummy GCLK, End GCLK1)
　　: GCLK10 → GCLK9 → GCLK8 → GCLK7 → GCLK6 → GCLK5 → GCLK4 →GCLK3 → GCLK2 → GCLK1.
　　4. In case of T5', If there is no abnormal display, no problem

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4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.
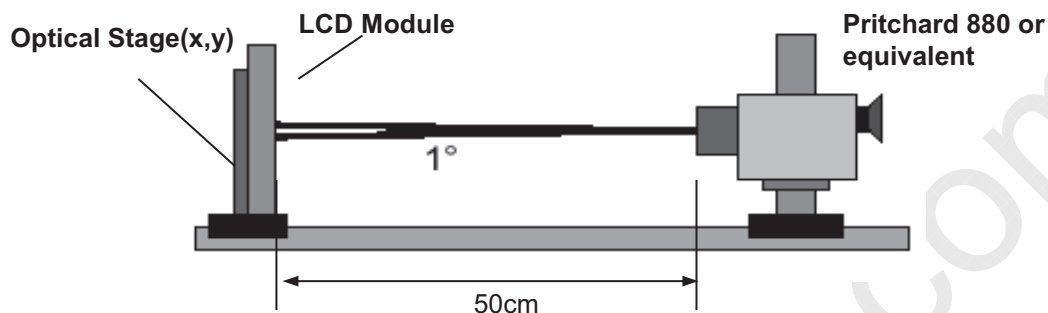

FIG. 1 Optical Characteristic Measurement Equipment and Method

Ta= 25±2°C, VDD,H_VDD,VGH,VGL=typ, fv=60Hz, BW=2.772Gbps, Light Source : D65 Standard

Table 6. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	850	1200	-		1
Response Time	Rising	Tr	-	8	12		2
	Falling	Tf	-	10	14	ms	
Transmittance		T	6.74	7.49		%	3
Color Coordinates [CIE1931]	RED	Rx		0.656			4
		Ry		0.327			
	GREEN	Gx	Typ -0.03	0.280	Typ +0.03		
		Gy		0.584			
	BLUE	Bx		0.134			
		By		0.130			
Viewing Angle (CR>10)							
	x axis, right(φ=0°)	θr	89	-	-	degree	5
	x axis, left (φ=180°)	θl	89	-	-		
	y axis, up (φ=90°)	θu	89	-	-		
	y axis, down (φ=270°)	θd	89	-	-		
Gray Scale			-	-	-		6

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Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.
The value of CR should be extracted using the LGD sheet structure (Diffuser/Prism/Prism)

※. Surface luminance is determined after the unit has been 'ON' and 1 Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white.
For more information see the FIG. 7.

2. Response time is the time required for the display to transit from G(0) to G(255) (Rising Time, Tr) and from G(255) to G(0) (Falling Time, Tf). For additional information, see the FIG. 8.

3. The value of transmittance should be extracted using the standard light source of D65
The value of Transmittance should be extracted using the LGD sheet structure (Diffuser/Diffuser).

4. The value of color coordinates should be extracted using the standard light source of D65

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 9.

6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 7.

Table 7. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.09
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L63	Gamma4
	L127	Gamma5
	L255	Gamma1
Negative Voltage	L255	Gamma18
	L127	Gamma14
	L63	Gamma13
	L0	Gamma10

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Measuring point for surface luminance & measuring point for luminance variation.

A : H / 9 mm
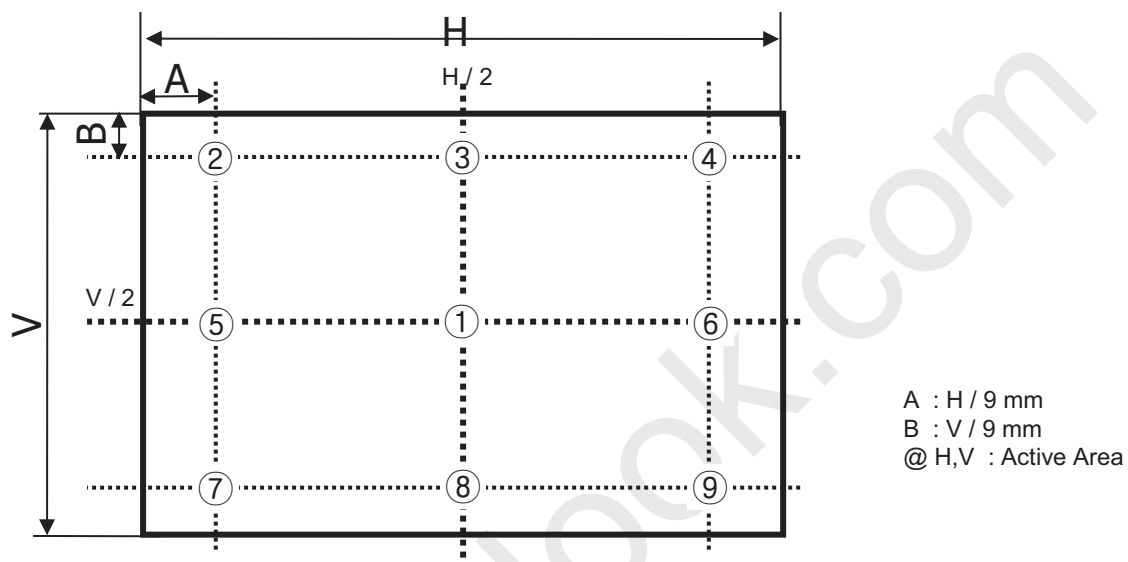B : V / 9 mm
@ H,V : Active Area

FIG. 7 9 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Black" ~ "White" and "White" ~ "Black".
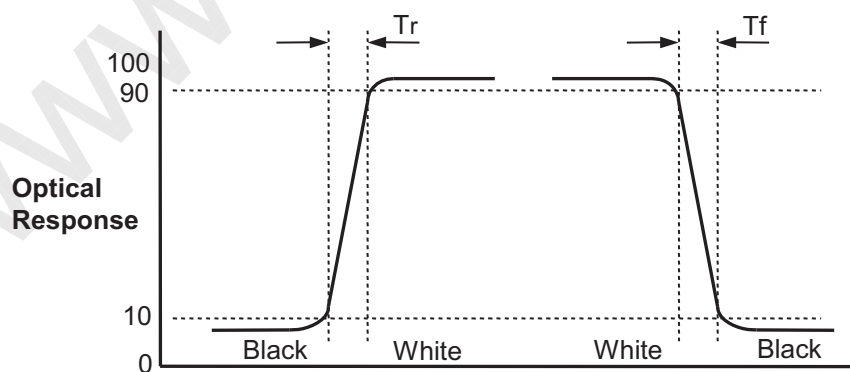

FIG. 8 Response Time

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Dimension of viewing angle range

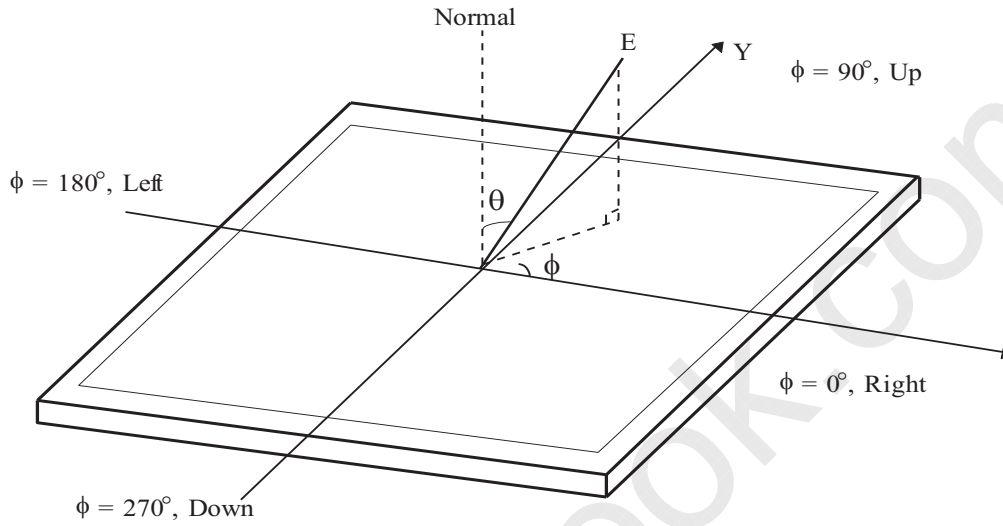**FIG. 9 Viewing Angle**

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5. Mechanical Characteristics

Table 8 provides general mechanical characteristics.

Table 8. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension (Only Glass)	Horizontal	1085.5 mm
	Vertical	617.7 mm
	Depth	1.2 mm
Active Display Area	Horizontal	1073.78 mm
	Vertical	604.00 mm
Weight	2.0Kg (Typ.)	
Surface Treatment	Hard coating(2H), Anti-glare low reflection treatment of the front polarizer (Haze 3%(Typ.))	

Note : Please refer to a mechanic drawing in terms of tolerance at the next page.

490D28-GLZX-02

14.8

14.8

1106.4

1076.9

19.8

303.5

607

641.6

14.8

51

40

318.3

40

30

30

22

22

16-M4

43.5

51

600

30

30

22

22

500

68.3

59.7

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6. Mechanical Dimension
6-1. Board Assembly Dimension

Date	Version

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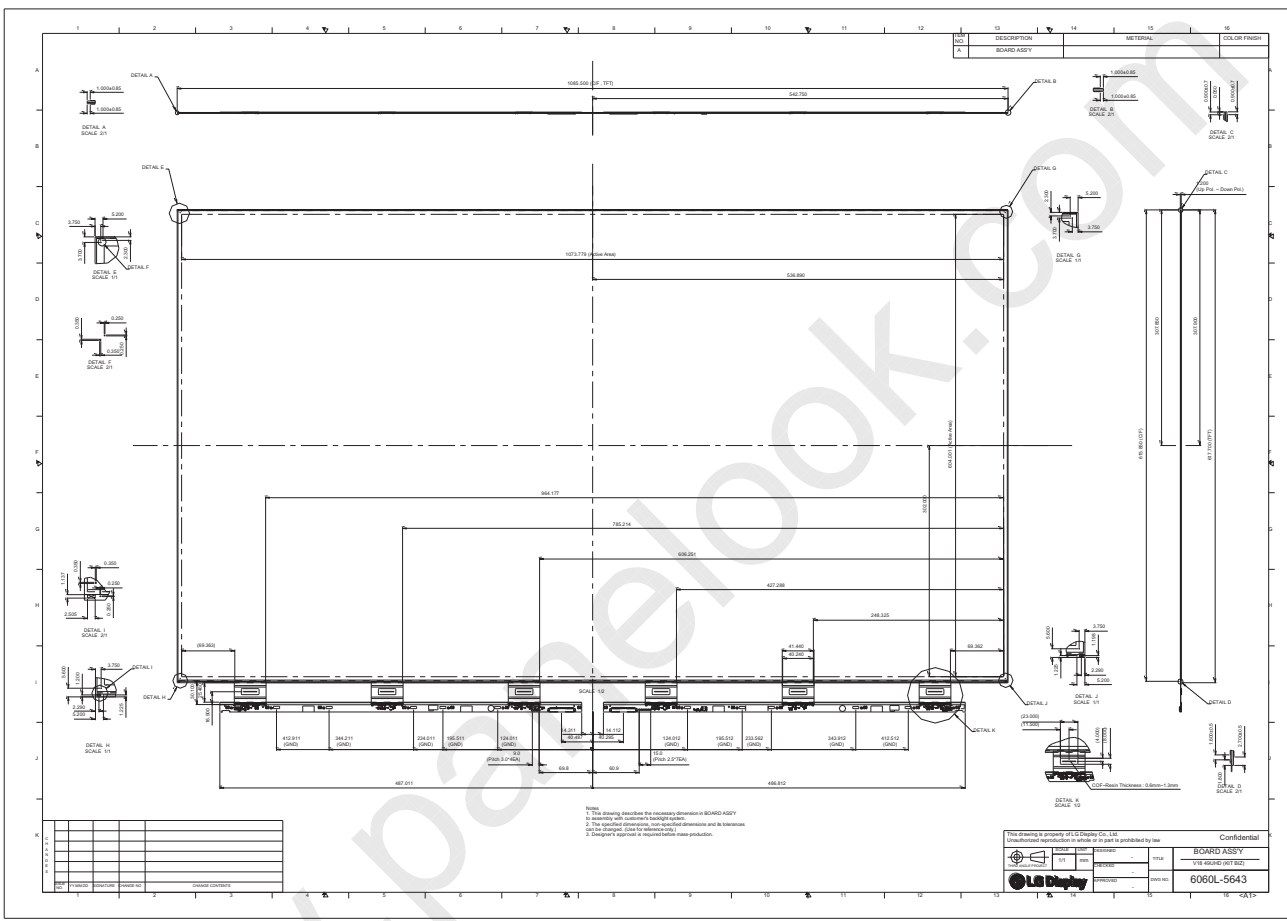
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7. Reliability

Table 9. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 90% 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 500h
4	Low temperature operation test	Ta= 0°C 500h
5	Humidity condition Operation	Ta= 40 °C ,90%RH
6	Altitude operating storage / shipment	0 - 16,400 ft 0 - 40,000 ft

Note : Before and after Reliability test, LCM should be operated with normal function.

Product Specification

8. International Standards

8-1. Safety

    a) UL 60065, Underwriters Laboratories Inc.
       Audio, Video and Similar Electronic Apparatus - Safety Requirements.

    b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
       Audio, Video and Similar Electronic Apparatus - Safety Requirements.

    c) IEC 60065, The International Electrotechnical Commission (IEC).
       Audio, Video and Similar Electronic Apparatus - Safety Requirements.

8-2. Environment

    a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

Product Specification

9. Packing

9-1. Information of B/Ass'y Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)   D : YEAR
E : MONTH   F ~ M : SERIAL NO.

notes

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the front side of the Left Source PCB.
This is subject to change without prior notice.

9-2. Packing Form

a) Package quantity in one Pallet : 168 pcs

b) Pallet Size : 1250mm(W) X 800mm(D) X 1120mm(H)

Product Specification

10. Precautions

Please pay attention to the followings when you use this TFT LCD module.

10-1. Handling Precautions

(1) Please attach the surface transparent protective film to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(2) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.

(3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)

(4) After removing the protective film, when the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(5) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(6) Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.

(7) Please make sure to avoid external forces applied to the Source PCB and D-IC during the process of handling or assembling the TV set. If not, It causes panel damage or malfunction.

(8) Panel and BLU should be protected from the static electricity. If not, it causes IC damage.

(9) Do not pull or fold the source D-IC which connect the source PCB and the panel.

(10) Panel(board ass'y) should be put on the BLU structure precisely to avoid mechanical impact.

(11) FFC Cable should be connected between System board and Source PCB correctly.

(12) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.

(13) Surface temperature of the Component on PCB should be controlled under 100℃ (D-IC : 110℃) with TV Set status
If not, problems such as IC damage or decrease of lifetime could occur.
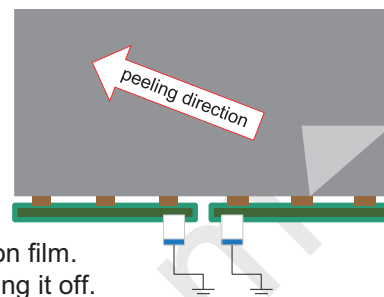
10-2. Operating Precautions

(1) Response time depends on the temperature.(In lower temperature, it becomes longer.)

(2) Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, Stable time(required time that brightness is stable after turned on) becomes longer

(3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

LC490DGJ

Product Specification

10-3. Protection Film

(1) Please keep attaching the protection film before assembly.
(2) Please peel off the protection film slowly.
(3) Please peel off the protection film just like shown in the Fig.1
(4) Ionized air should be blown over during the peeling.
(5) Source PCB should be connected to the ground when peel off the protection film.
(6) The protection film should not be contacted to the source D-IC during peeling it off.

peeling direction

< Fig. 1 >

10-4. Storage Precautions

When storing modules as spares for a long time, the following precautions are necessary.

(1) Temperature : 5 ~ 40 ℃
(2) Humidity : 35 ~ 75 %RH
(3) Period : 6 months
(4) Control of ventilation and temperature is necessary.
(5) Please make sure to protect the product from strong light exposure, water or moisture. Be careful for condensation.
(6) Please keep the modules at a circumstance shown below Fig. 2

No Baking	50℃, 10%, 24hr	50℃, 10%, 48hr
2 month	3 month	6 month

< Fig. 2 >

10-5. Packing Precautions

Product assembled into module should be stored in the Al-bag(cover case).
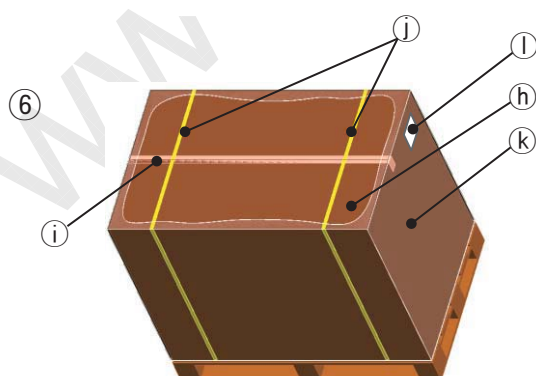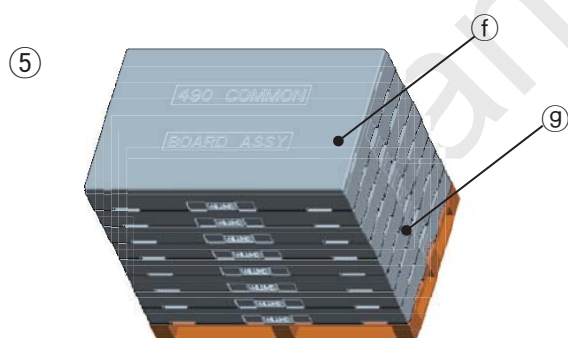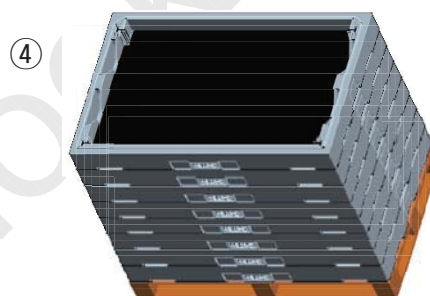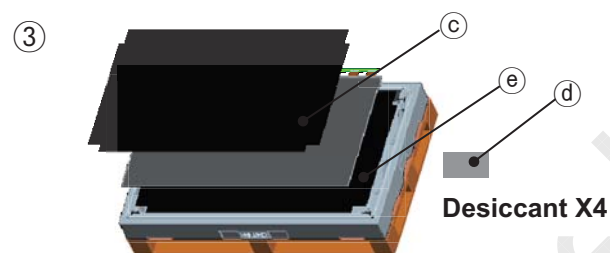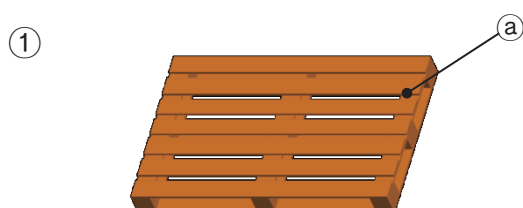
Ver. 1.0

LC490DGJ

Product Specification

APPENDIX-Ⅰ-1

■ Pallet Ass'y

  a) B/Ass'y Qty + PE Sheet / Box : 21pcs + 22pcs
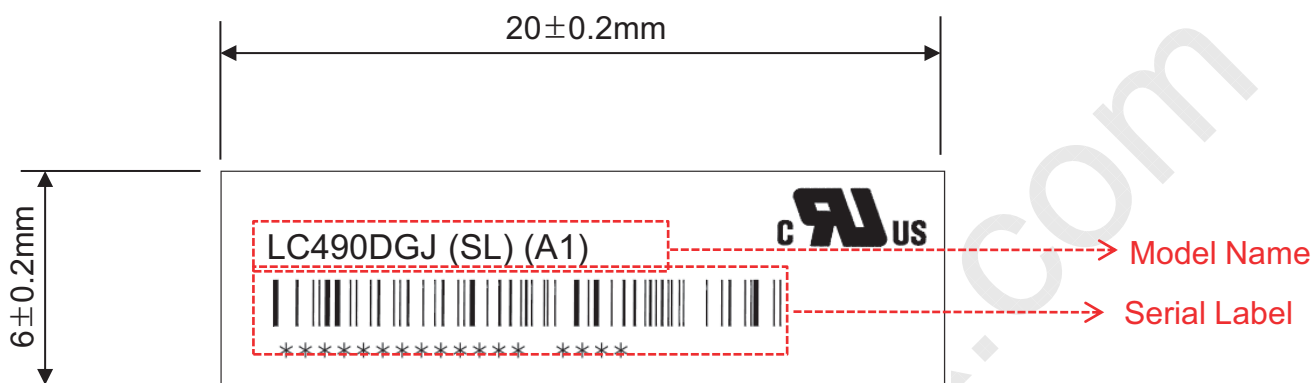 b) B/Ass'y Qty / Pallet : 168pcs
  c) Box Qty / Pallet : 8Box

Desiccant X4

No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	Carton Plate	Paper(SW)
ⓒ	PE Sheet	LDPE
ⓓ	Desiccant	Power dry
ⓔ	AL-Sheet	Aluminum
ⓕ	Top Packing	EPS
ⓖ	Bottom Packing	EPS
ⓗ	Angle Packing	Paper(SW)
ⓘ	Tape	OPP
ⓙ	Band	PP
ⓚ	Wrap	L-LDPE
ⓛ	Label	PP

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Product Specification

APPENDIX-Ⅱ-1

■ Serial Label

20±0.2mm

6±0.2mm

LC490DGJ (SL) (A1)

************* ****

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Model Name

Serial Label

■ Serial No. (See CAS page 22 for more information)
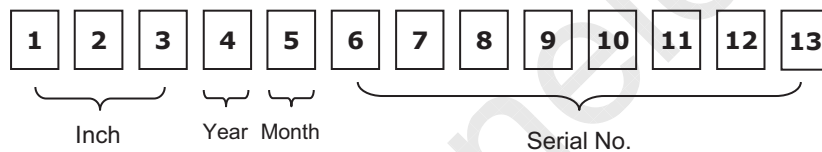
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |

Inch   Year   Month   Serial No.

Ver. 1.0

Product Specification

APPENDIX-Ⅱ-2

■ BOX Label

M2D8CA00002MB

LC490DGJ-SLA1
 QTY : 21

Grade:A

(label width 75.0, height 45.0)

■ Pallet Label

LC490DGJ
SLA1

168 PCS	001/01-01	
MADE IN CHINA		RoHS Verified

XXXXXXXXXXXXX XXX

(label width 100.0, height 70.0)
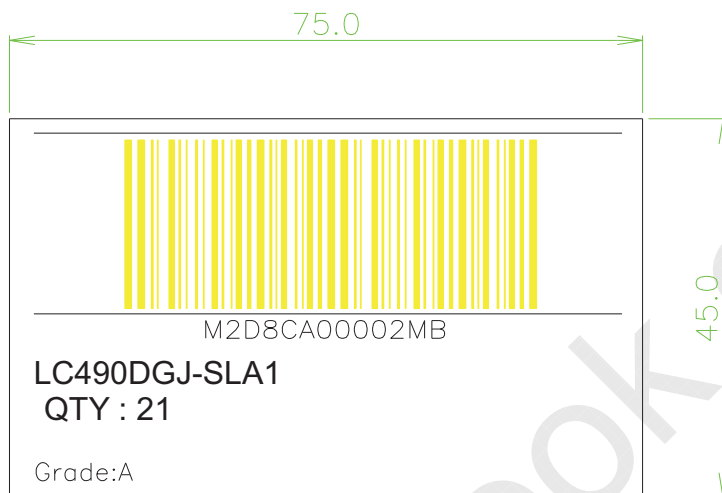
LC490DGJ

Product Specification

APPENDIX- III

■ Source D-IC Power Sequence

Case1

(1) (1) (2) (2) (1) (1)

VDDH　　　　　VDDH

GMA1 ~ GMA18　　GMA1 ~ GMA18

HVDD　　　　　HVDD

0.5VDDH　　　　　　　　0.5VDDH
0.5(GMA1 ~ GMA18)　　　　　0.5(GMA1 ~ GMA18)
0.5HVDD　　　　0.5HVDD

VCCA/D　　　　　VCCA/D

0.5VCCA/D　　　　　　　　　　　0.5VCCA/D

Input Signal　Input Signal
Vterm　　　Vterm

GND　　　　　　　　　　　　　GND

Note : (1)=0~1s, (2)=-200ms~1s (Always, VDD must be higher than or same width HVDD.)

Case2

(1) (3) (1) (1) (3) (2)

VDDH　　　　　VDDH

GMA1 ~ GMA18　　GMA1 ~ GMA18

HVDD　　　　　HVDD

0.5VDDH　　　　　　　　0.5VDDH
0.5(GMA1 ~ GMA18)　　　　　0.5(GMA1 ~ GMA18)
0.5HVDD　　　　0.5HVDD

VCCA/D　　　　　VCCA/D

0.5VCCA/D　　　　　　　　　　　0.5VCCA/D

Input Signal　Input Signal
Vterm　　　Vterm

GND　　　　　　　　　　　　　GND

Note : (1)=0~1s, (2)=-200ms~1s,

(3)=-200ms~1s (Always, VDD must be higher than or same width HVDD.)

- Input Signal : EPI

LC490DGJ

Product Specification

APPENDIX- IV

■ The reference method of BL dimming

It is recommended to use synchronous V-sync frequency to prevent waterfall
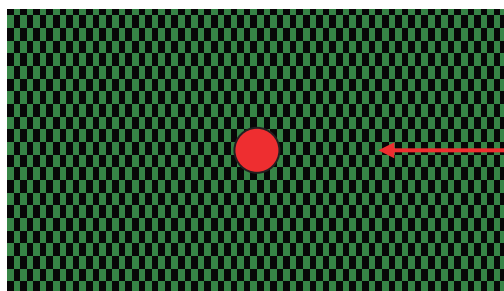(Vsync * 2 =P-Dim Frequency)

Ver. 1.0   27/28
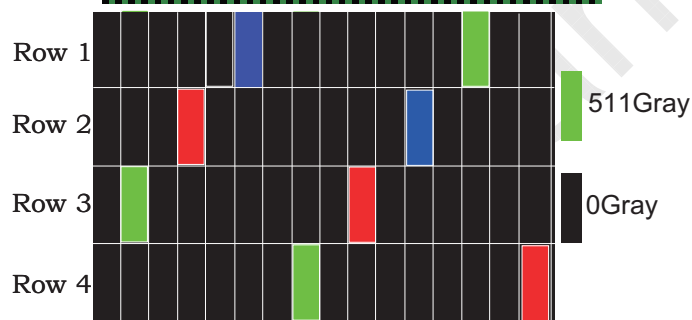
LC490DGJ

Product Specification

APPENDIX- V

■ Flicker Adjustment

1) Mplus mode must be RGB Mode for flicker adjustment

Parameter	Unit	Min	Typ	Max	Note
Inversion Method	-	V4-Dot Inversion			
Adjust Pattern / Gray Level	-	V4Dot Full Flicker / 511Gray			60Hz
Position	-	Center			
Voltage range	V	3.72	4.22	4.72	

Tune the V-com level till the flicker level became stable on center position.

Row 1

Row 2   511Gray

Row 3   0Gray

Row 4

[Input data]

Row 1

Row 2   511Gray

Row 3   0Gray

Row 4
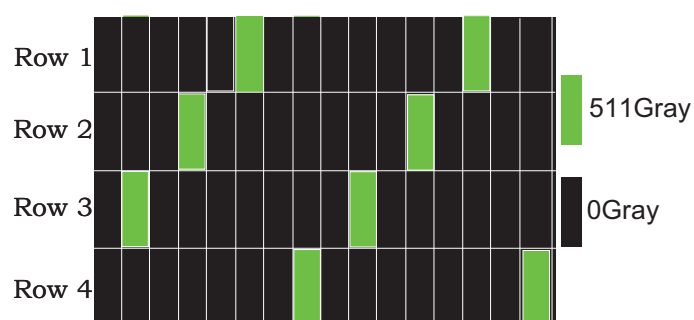
[M+ Panel]

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Product Specification

APPENDIX - Ⅵ

■ EQ Mode

1. EPI EQ Option

Tab	#1	#2	#3	#4	#5	#6
EQ 정보	LH	LH	LH	LH	LH	LH
Pre-Emp	48%	48%	24%	24%	48%	48%

Ver. 1.0